ABSTRACT

A method is provided to reduce clock skew in an integrated circuit having a number of circuit blocks, which comprises the following steps. A first source clock coupled to a clock input terminal of a first circuit block within the circuit blocks is provided, as is a second source clock coupled to a clock input terminal of a second circuit block within the circuit blocks. When the second circuit block is configured to operate in synchronization with the first circuit block, the clock input terminal of the second circuit block is switched to the first source clock, and thus both the first circuit block and the second circuit block can operate in accordance with the same first source clock.